

Attorney Docket Number 40704/DMC/F179

Application Number 09/851,708

Filing Date May 8, 2001

Applicant(s) Indradeep Ghosh

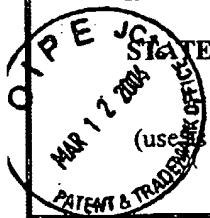
Group Art Unit 2133

Examiner Name R. Stephen Dildine, Jr.

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)



U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE
RGD		5,748,647	05-05-1998	Bhattacharya, et al.
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)

OTHER DOCUMENTS

RGD	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RGD	European Search Report dated 19 January 2004 for European Application No. EP 01304884.1-2216, Search Report mailed February 23, 2004 (4 pgs.)
RGD	Ghosh et al., "Automatic Test Pattern Generation for Functional RTL Circuits Using Assignment Decision Diagrams," Design Automation Conference, (IEEE CAT. No. 00CH37106), Proceedings 2000 of ACM/IEEE-CAS/EDAC Design Automation Conference, Los Angeles, California, June 5-9, 2000 (p 43-48).
RGD	Jervan et al., "High-Level Test Synthesis With Hierarchical Test Generation," Proceedings '99 17th Norchip Conference, Oslo, Norway, Nov. 8-9, 1999 (p 291-296).
RGD	Ubar et al., "Efficient Hierarchical Approach to Test Generation for Digital Systems," Tallin Technical University Conference Proceeding, 20 March 2000 (p 189-195).
RGD	Vandeveenter et al., "Using Binary Decision Diagrams to Speed Up the Test Pattern Generation of Behavioral Circuit Descriptions Written in Hardware Description Languages," Circuits and Systems, 1994 IEEE International Symposium On London, UK, May 30-June 2, 1994 (p 279-282).

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EXAMINER SIGNATURE	DATE CONSIDERED
<i>R. Stephen Dildine</i>	8/6/04

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